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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,671	04/23/2001	Katsuaki Matsui	32011-171408	1009

7590 10/28/2003  
Volentine Francos, PLLC  
12200 Sunrise Valley Drive  
Suite 150  
Reston, VA 20191

EXAMINER

WEST, JEFFREY R

ART UNIT	PAPER NUMBER
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2857

DATE MAILED: 10/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/839,671

Applicant(s)

MATSUI, KATSUAKI

Examiner

Jeffrey R. West

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 July 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 21-42 is/are pending in the application.
- 4a) Of the above claim(s) 26-42 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 21-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 22 April 2003 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The Examiner does point out that Applicant's priority document contains six figures and a corresponding description of Figure 6 as conventional in the art. The instant application, however, does not contain a Figure 6 or the corresponding description (See JP Publication No. 2002-033455 and the corresponding translation provided).

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,393,592 to Peeters et al. in view of JP Patent No. 61-016615 to Kato.

Peeters discloses scan flop circuitry and methods for making the same comprising a circuit block for connection to previous circuit blocks in a scan chain (column 4, lines 20-24) including a circuit block in which an input signal is input at a

timing in accordance with an input clock and which outputs an output signal having a value corresponding to said input signal comprising a first signal path for guiding a test input signal to a signal input terminal of the circuit block, a second signal path for guiding a clock to a clock input terminal of the circuit block, and a third signal path for guiding an output signal (Figure 3). Peeters also discloses a selector on the first signal path which, during normal operation, supplies an output signal from a preceding circuit block to the input terminal of the circuit block and which during a test operation supplies the test input signal to the signal input terminal of the circuit block as well as a selector on the second signal path which, during normal operation supplies a normal clock to the input terminal of the circuit block and during a test operation supplies a test clock to the clock input terminal of the circuit block (Figure 3 and column 4, lines 21-39). Peeters also discloses the conventional method of receiving and outputting the signals via test pads (Figure 1B, "SI", "CLK", and "SO").

While Peeters does teach many of the features of the claimed invention, Peeters does not specifically disclose signal paths from the clock to an output pad and the terminal output to an output pad having substantially equal wiring delay time.

Kato teaches a circuit block to which an input signal is input at a timing in accordance with an input clock and which outputs an output signal having a value corresponding to said input signal (Figures 3 and 4) a first signal path for guiding an input signal, which has been supplied to a first pad (Figure 3, "1"), to a signal input terminal of the circuit block (Figure 3, "10"), a second signal path for guiding a clock, which has been supplied to a second pad (Figure 3, "2"), to a clock input terminal of

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the circuit block (Figure 3, "8"), a third signal path for guiding an output signal, which has been output from a signal output terminal of the circuit block, to a third pad (Figure 3, "6"), a fourth signal path for guiding the clock, which is input to the clock input terminal, to a fourth pad (Figure 3, "7"), wherein the third and fourth signal paths are formed so that wiring delay time of the third and fourth signal paths are substantially equal (abstract).

It would have been obvious to one having ordinary skill in the art to modify the invention of Peeters to include signal paths from the clock to an output pad and the terminal output to an output pad having substantially equal wiring delay time, as taught by Kato, because Peeters discloses connecting the circuit block in a scan chain (column 4, lines 20-24), but in this configuration it is considered inherent that a delay will occur between the time a second circuit block receives an output from the previous circuit block and the time the second circuit block receives a clock input, since the clock does not pass through any other blocks. Therefore, the combination of Peeters and Kano, as suggested by Kano, would have eliminated this delay when the circuit block responds to a frequency nearly as high as the frequency of the clock signal, even in cases of changing operating conditions, in order to maintain proper operation (abstract).

4. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peeters in view of Kato, and further in view of U.S. Patent No. 6,615,380 to Kapur et al.

As noted above, the invention of Peeters and Kato teaches all the features of the claimed invention except for providing selectors on the third and fourth signal paths in order to supply a test output during test operation and a non-test output during normal operation.

Kapur teaches dynamic scan chains and test pattern generation methodologies comprising a plurality of circuit blocks connected in a scan chain wherein the path for guiding the test output signal from a signal output terminal includes a selector which supplies a test signal during testing and a normal output during normal operation (Figure 4 and column 2, lines 24-33).

It would have been obvious to one having ordinary skill in the art to modify the invention of Peeters and Kato to include providing a selector on the third signal path in order to supply a test output during test operation and a non-test output during normal operation, as taught by Kapur, because, as suggested by Kapur, the combination would have provided a method for selectively bypassing circuits during testing in order to use shorter test patterns resulting in a reduction in overall test data volume and test application time with the same quality of results (column 2, lines 24-33).

Although the combination of Peters, Kato, and Kapur does not specifically disclose a selector on the fourth path (i.e. clock-to-out path) one having ordinary skill in the art would have been motivated to include such a selector since the combination of Peters, Kato, and Kapur teaches maintaining substantially no delay between the third and fourth paths and placing a selector on both the third and fourth

paths, instead of just the third path, would have insured that the signals on these two paths bypass the same sections of circuitry thereby maintaining equivalency.

### ***Response to Arguments***

5. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,774,474 to Narayanan et al. teaches pipelined scan enable for fast scan testing.

U.S. Patent No. 5,923,676 to Sunter et al. teaches BIST architecture for measurement of integrated circuit delays including an input selector.

U.S. Patent No. 5,430,394 to McMinn et al. teaches a configuration and method for testing a delay chain within a microprocessor clock generator.

U.S. Patent No. 6,308,291 to Kock et al. teaches a method for testing an electronic circuit.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jr  
October 17, 2003

  
MARC S. HOFF  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800